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ART UNIT	**PAPER NUMBER**
2123	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/630,348	HSU ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-19 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on July 31, 2000 together with copies of the patents and papers. The patents and papers have been considered.

Drawings

3. The drawings submitted on July 31, 2000 are accepted.

Specification

4. The disclosure is objected to because of the following informalities:

Page 5, Lines 3-4, "representing the state of any each signal that may be included" appears to be incorrect and it appears that it should be "representing the state of any signal that may be included".

Page 5, Lines 7-8, "state of the simulation circuit forms the $STATE_0$ input variable" appears to be incorrect and it appears that it should be "state of the simulation circuit forms the $STATE_0$ of the input variable".

Page 8, Lines 10-11, "The RESET signal is then set true (R) with the count signal is set to false" appears to be incorrect and it appears that it should be "The RESET signal is then set true (R) and the count signal is set to false".

Page 12, Lines 6-7, "The model of FIG. 2 similarly defines all transitions from states 2-7" appears to be incorrect and it appears that it should be "The model of FIG. 3 similarly defines all transitions from states 2-7".

Page 14, Lines 16-17, "that might within the time allotted for the consequent behavior" appears to be incorrect and it appears that it should be "that might occur within the time allotted for the consequent behavior".

Page 17, Line 1, "current state of the simulate circuit" appears to be incorrect and it appears that it should be "current state of the simulation circuit".

Page 18, Lines 34-35, "do not need to represents" appears to be incorrect and it appears that it should be "do not need to represent".

Page 20, Line 31, "Thus is not necessary for function" appears to be incorrect and it appears that it should be "Thus it is not necessary for function".

Page 21, Lines 13-14, "investigate function response to only 2_5 (32) input variable combinations instead of 2_{21} (2,097,152) possible input variable combinations" appears to be incorrect and it appears that it should be "investigate function response to only 2^5

(32) input variable combinations instead of 2^{21} (2,097,152) possible input variable combinations".

Page 22, Lines 14-16, It is not clear as to what the applicants wanted to say in "Thus has been shown and described a system for verifying that a circuit specification describes a circuit that a specification will exhibit a particular property". Rewording this sentence is requested.

The specification and the claims have been prepared in 1½ line spacing. The spacing of the lines of the specification is such as to make reading and entry of amendments difficult. A new specification incorporating all the aforementioned corrections with lines double spaced on good quality paper are required. No new matter may be added.

Appropriate corrections are required.

Claim Objections

5. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

6. Claims 6, 7 and 10-13 are objected to because of the following informalities:

Claim 6, Lines 31-34, "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern" appears to be

incorrect and it appears that it should be "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern".

Claim 10, Lines 34-37, "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern" appears to be incorrect and it appears that it should be "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern".

Claims objected to but not specifically addressed are objected to based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 9-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation " The apparatus in accordance with claim 8 " in Line 27 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 8 refers to "A method for verifying" and not an apparatus.

Claim 10 recites the limitation " The apparatus in accordance with claim 9 " in Line 33 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 9 refers to "The apparatus in accordance with claim 8", but Claim 8 refers to "A method for verifying" and not an apparatus.

Claim 11 recites the limitation " The apparatus in accordance with claim 10 " in Line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim, as the base claim 8 refers to "A method for verifying" and not an apparatus.

Claim 11 recites the limitation " further comprising means for receiving and analyzing " in Lines 1-2 of the claim. This is incorrect as claim 11 is a method claim and therefore cannot contain means for, but will comprise steps.

Claim 12 recites the limitation " The method in accordance with claim 11 " in Line 6 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 11 refers to "The apparatus in accordance with claim 10" and not an apparatus.

Claim 13 recites the limitation " The apparatus in accordance with claim 12 " in Line 12 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 12 refers to "The method in accordance with claim 11" and not an apparatus.

Claim 16 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 15. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Interpretations

9. For the purpose of art rejections, the objected to and rejected claims have been interpreted as follows:

In Claim 6, Lines 31-34, "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern" is interpreted as "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern".

In Claim 9 the limitation "The apparatus in accordance with claim 8" in Line 27 of the claim is interpreted as "The method in accordance with claim 8".

In Claim 10 the limitation " The apparatus in accordance with claim 9" in Line 33 of the claim is interpreted as "The method in accordance with claim 9".

In Claim 10, Lines 34-37, "the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle k that are included in the second state change pattern" is interpreted as "the Kth circuit function CKT_K

(for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern".

In Claim 11 the limitation " The apparatus in accordance with claim 10 " in Line 1 of the claim is interpreted as "The method in accordance with claim 10".

In Claim 11 the limitation "further comprising means for receiving and analyzing" in Lines 1-2 of the claim is interpreted as "further comprising the steps of receiving and analyzing"

In Claim 13 the limitation " The apparatus in accordance with claim 12 " in Line 12 of the claim is interpreted as "The method in accordance with claim 12".

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya (KA)** (U.S. Patent 5,905,883) in view of **Cheng et al. (CH)** (U.S. Patent 5,513,122).

12.1 **KA** teaches verification system for circuit simulator. Specifically as per Claim 1, **KA** teaches a method for verifying that a circuit described by a circuit specification as receiving and processing input signals to produce output signals has a property of responding to a first pattern in its input signals by producing a second pattern in its output signals within a finite time the method (Abstract; Fig1, Items104, 106, 136, 140, 146, 148, 150, 102, 112 and 120; Fig. 3A and 3B; CL2, L54-60); comprising the step of:

(a) simulating operation of the circuit described by the circuit specification to produce output waveform data representing behavior of the circuit's input and output signals and representing a state of the circuit, wherein the output waveform data represents at least one occurrence of the first pattern in the input signals (Abstract; Fig 1, Items 106, 112, 140 and 150).

KA teaches determining the output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals (Abstract; Fig 1, Items 136, 146, 148, 150, 140 and 158). **KA** does not expressly teach determining a current state of the circuit from the output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals (step b). **CH** teaches determining a current state of the circuit from the output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals (Abstract, L6-11 and L14-15), as that provides the initial

configurations of the states and variable values (Abstract, L6-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **CH** that included determining a current state of the circuit from the output waveform data whenever the output waveform data represents an occurrence of the first pattern in the input signals, as that would provide the initial configurations of the states and variable values.

KA teaches processing the circuit specification to determine whether starting from each initial waveform determined in step b, the circuit it describes will exhibit the second pattern within that finite time under all possible combinations of input signal waveform during the finite time (Abstract; Fig 1, Items 106, 116, 136, 140, 146, 148, 150; Fig. 3A & 3B; CL2, L54-60). **KA** does not expressly teach processing the circuit specification to determine whether starting from each current state determined in step b, the circuit it describes will exhibit the second pattern within that finite time under all possible combinations of input signal states during the finite time (step b). **CH** teaches processing the circuit specification to determine whether starting from each current state determined in step b, the circuit it describes will exhibit the second pattern within that finite time under all possible combinations of input signal states during the finite time (Abstract, L6-11 and L14-15), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **CH** that included processing the circuit specification to determine whether starting

from each current state determined in step b, the circuit it describes will exhibit the second pattern within that finite time under all possible combinations of input signal states during the finite time, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

12.2 As per Claim 14, **KA** teaches an apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals (Abstract; Fig1, Items104, 106, 136, 112, 150, 146, 148); the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification (Abstract, L1-2; Fig1, Items 106, 112);

wherein the circuit simulator produces output waveform data representing time varying behavior of the input and output signals and representing a current state of the simulated circuit (Abstract, L10-17);

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event (Fig1, Items 136, 150, 146, 148; CL2, L54-60); and

circuit output represented by the circuit simulator output waveform data when the detector means detects the data pattern representing the antecedent event (Fig1, Items 136, 150, 146, 148).

KA does not expressly teach the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state

change pattern in at least one of the output signals. **CH** teaches the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals (Abstract, L6-11 and L14-15), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **CH** that included the antecedent event being a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior was a second state change pattern in at least one of the output signals, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

KA does not expressly teach means for generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit. **CH** teaches means for generating a state space model of the simulated circuit representing states of the simulated circuit that are reachable from the current state of the simulated circuit (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

apparatus of **KA** with the apparatus of **CH** that included means for generating a state space model of the simulated circuit representing states of the simulated circuit that would be reachable from the current state of the simulated circuit, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

KA does not expressly teach means for analyzing the state space model to verify the circuit exhibits the consequent behavior. **CH** teaches means for analyzing the state space model to verify the circuit exhibits the consequent behavior (Abstract, L8-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **CH** that included means for analyzing the state space model to verify the circuit exhibits the consequent behavior, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

13. Claims 2-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya (KA)** (U.S. Patent 5,905,883) in view of **Cheng et al. (CH)** (U.S. Patent 5,513,122), and further in view of **Ganesan et al. (GA)** (U.S. Patent 6,138,266).

13.1 As per Claim 2, **KA** teaches an apparatus for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior occurring during clock cycles 1 - N of a clock signal following an antecedent event, wherein N is an integer greater than 0, wherein the circuit responds to input signals by producing output signals (Abstract; Fig1, Items104, 106, 136, 112, 150, 146, 148); the apparatus comprising:

a circuit simulator for implementing a simulated circuit, wherein the simulated circuit simulates the circuit described by the circuit specification (Abstract, L1-2; Fig1, Items 106, 112);

wherein the circuit simulator produces output waveform data representing time varying behavior of the input and output signals and representing a current state of the simulated circuit (Abstract, L10-17); and

detector means for detecting in the output waveform data an occurrence of a data pattern representing the antecedent event (Fig1, Items 136, 150, 146, 148; CL2, L54-60).

KA does not expressly teach the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals. **CH** teaches the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is production of a second state change pattern in at least one of the output signals (Abstract, L6-11 and L14-15), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary

skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **CH** that included the antecedent event being a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior was production of a second state change pattern in at least one of the output signals, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

KA does not expressly teach means for generating a temporally expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles. **GA** teaches means for generating a temporally expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles (Fig. 2; CL2, L25-50; Fig 17A; CL24, L15-64), as that allows the circuit to be divided into a plurality of blocks and truth tables for the blocks to be computed and stored in memory, so output values can be computed quickly (Abstract, L2-10; CL2, L32-34; CL2, L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **GA** that included means for generating a temporally expanded model of the simulated circuit representing the circuit as a set of N circuit functions CKT_1-CKT_N, each corresponding to a separate one of the N clock cycles, as that would allow the circuit to be divided into a plurality of blocks and truth tables for the blocks to be computed and stored in memory, so output values could be computed quickly.

13.2 As per Claim 3, **KA, CH** and **GA** teach the apparatus of claim 2. **KA** does not expressly teach that the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior. **GA** teaches that the Kth circuit function CKT_K (for K = 1 to N) has a first input variable representing states of circuit input signals at a start of clock cycle K that influence the consequent behavior (Fig 2, Blks 210 and 201), as that allows generating output data values of a target design corresponding to the input data values (primary inputs) provided from outside (CL2, L35-38). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **GA** that included the Kth circuit function CKT_K (for K = 1 to N) having a first input variable representing states of circuit input signals at a start of clock cycle K that influenced the consequent behavior, as that would allow generating output data values of a target design corresponding to the input data values (primary inputs) provided from outside.

13.3 As per Claim 4, **KA, CH** and **GA** teach the apparatus of claim 3. **KA** does not expressly teach that the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior. **GA** teaches that the Kth circuit function CKT_K (for K = 1 to N) has a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior (Fig 2, Blks 220 and 234; CL2, L42-43), as that allows using the outputs of some blocks from one cycle to be used as inputs to some other blocks in a subsequent cycle based on the dependencies dictated by the target design (CL2, L43-45). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **GA** that included the Kth circuit function CKT_K (for K = 1 to N) having a second input variable representing states of circuit output signals at the start of clock cycle K that influence the consequent behavior, as that would allow using the outputs of some blocks from one cycle to be used as inputs to some other blocks in a subsequent cycle based on the dependencies dictated by the target design.

13.4 As per Claim 5, **KA, CH** and **GA** teach the apparatus of claim 4. **KA** does not expressly teach that the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior. **GA** teaches that the Kth circuit function CKT_K (for K = 1 to N-1) has a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior (Fig 2, Item 291; CL7, L39-40), as the output values of the IC can be determined by evaluating the circuit functions (Abstract, L6-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **GA** that included the Kth circuit function CKT_K (for K = 1 to N-1) having a first output variable representing states of circuit output signals at an end of clock cycle K that influence the consequent behavior, as the output values of the IC could be determined by evaluating the circuit functions.

13.5 As per Claim 6, **KA, CH** and **GA** teach the apparatus of claim 5. **KA** does not expressly teach that the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable

representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern. **GA** teaches that the Kth circuit function CKT_K (for K = 1 to N-1) has a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern (Fig 2, Blk 234; CL2, L42-43), as that allows using the outputs of some blocks from one cycle to be used as inputs to some other blocks in a subsequent cycle based on the dependencies dictated by the target design (CL2, L43-45). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **GA** that included the Kth circuit function CKT_K (for K = 1 to N-1) having a second output variable representing states of any circuit output signals at the end of clock cycle K that are included in the second state change pattern, as that would allow using the outputs of some blocks from one cycle to be used as inputs to some other blocks in a subsequent cycle based on the dependencies dictated by the target design.

13.6 As per Claim 7, **KA, CH** and **GA** teach the apparatus of claim 6. **KA** does not expressly teach means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior. **GA** teaches means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibits the consequent behavior (CL7, L57-62), as that allows verification of cycle based designs treating target design as a combinatorial logic (truth table) receiving several primary inputs and generating several combinatorial logic outputs (CL7, L55-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

apparatus of **KA** with the apparatus of **GA** that included means for receiving and analyzing the second output variable of each of the circuit functions to verify whether the circuit exhibited the consequent behavior, as that would allow verification of cycle based designs treating target design as a combinatorial logic (truth table) receiving several primary inputs and generating several combinatorial logic outputs.

13.7 As per Claims 8-13, these are rejected based on the same reasoning as Claims 2, 5-7, 3 and 4, supra. Claims 8-13 are method claims reciting the same limitations as Claims 2, 5-7, 3 and 4, as taught throughout by **KA, CH** and **GA.**

14. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya (KA)** (U.S. Patent 5,905,883) in view of **Cheng et al. (CH)** (U.S. Patent 5,513,122), and further in view of **Selvidge et al. (SE)** (U.S. Patent 6,009,531).

14.1 As per Claim 15, **KA** and **CH** teach the apparatus of claim 14. **KA** teaches that the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event (Abstract, L13-17; Cl2, L54-60).

KA does not expressly teach that the circuit transitions between states only on edges of a periodic clock signal supplied as input. **SE** teaches that the circuit transitions between states only on edges of a periodic clock signal supplied as input (CL8, L4-11 and L22-29; Cl9, L60-65), as that would allow the user to control the precise time of sampling signals from the target system by properly connected storage devices (CL10, L37-40). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **KA** with the apparatus of **SE** that included the circuit transitioning between states only on edges of a periodic clock signal supplied as input, as that would allow the user to control the precise time of sampling signals from the target system by properly connected storage devices.

KA teaches the circuit simulator output data generated within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event (Abstract, L13-17; Cl2, L54-60). **KA** does not expressly teach the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event. **CH** teaches the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the apparatus of **KA** with the apparatus of **CH** that included the state space model representing all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

14.2 As per Claim 16, **KA, CH** and **SE** teach the apparatus of claim 15. **KA** teaches the circuit simulator output data generated within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event (Abstract, L13-17; Cl2, L54-60). **KA** does not expressly teach the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data within the finite number of clock signal cycles after the detector means detects the data pattern representing the antecedent event. **CH** teaches the state space model represents all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the apparatus of **KA** with the apparatus of **CH** that included the state space model representing all states of the simulated circuit that are reachable from the current state of the simulated circuit represented by the circuit simulator output data, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

15. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya (KA)** (U.S. Patent 5,905,883) in view of **Cheng et al. (CH)** (U.S. Patent 5,513,122), and further in view of **Baumgartner et al. (BA)** (U.S. Patent 6,449,752).

15.1 As per Claim 17, **KA** teaches a method for verifying that a circuit specification describes a circuit exhibiting a property defined as a consequent behavior following an antecedent event, wherein the circuit responds to input signals by producing output signals (Abstract; Fig1, Items104, 106, 136, 112, 150, 146, 148); and

circuit output represented by the waveform data when the data represents the antecedent event (Fig1, Items 136, 150, 146, 148).

KA does not expressly teach the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals. **CH** teaches the antecedent event is a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior is a second state change pattern in at least one of the output signals (Abstract, L6-11 and L14-15), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **CH** that included the antecedent event being a first state change pattern in at least one of the input and output signals, and wherein the consequent behavior was a second state change pattern in at least one of

the output signals, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

KA does not expressly teach simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit. **BA** teaches simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit (CL6, L23 to CL7, L14), as that would allow evaluating state changes on each next cycle and determining if there is any possible transition to a next state in any cycle in the future (CL6, L43-48). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **BA** that included simulating the circuit to produce waveform data representing successive state changes of the input and output signals and representing successive states of the circuit, as that would allow the user to determine if a given specification produced unexpected results; and allow evaluating state changes on each next cycle and determining if there is any possible transition to a next state in any cycle in the future.

KA does not expressly teach generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit represented by the waveform data when the data represents the antecedent event. **CH** teaches generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design

of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **KA** with the method of **CH** that included generating a state space model of the circuit including states of the circuit that are reachable from a state of the circuit, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

KA does not expressly teach analyzing the state space model to verify the circuit exhibits the consequent behavior. **CH** teaches analyzing the state space model to verify the circuit exhibits the consequent behavior (Abstract, L8-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **CH** that included analyzing the state space model to verify the circuit exhibits the consequent behavior, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

15.2 As per Claim 19, **KA, CH** and **BA** teach the method of claim 17. **KA** teaches the circuit output generated by the waveform data within the finite number of periods of the clock signal

after the waveform data represents the antecedent event (Abstract, L13-17; Cl2, L54-60). **KA** does not expressly teach the generated state space model includes only states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event. **CH** teaches the generated state space model includes only states of the circuit that are reachable from the current state of the circuit (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **KA** with the method of **CH** that included the generated state space model including only states of the circuit that would be reachable from the current state of the circuit, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

16. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kasuya (KA)** (U.S. Patent 5,905,883) in view of **Cheng et al. (CH)** (U.S. Patent 5,513,122), and further in view of **Baumgartner et al. (BA)** (U.S. Patent 6,449,752) and **Selvidge et al. (SE)** (U.S. Patent 6,009,531).

16.1 As per Claim 18, **KA, CH** and **BA** teach the method of claim 17. **KA** teaches that the consequent behavior occurs during a finite number of periods of the clock signal following the antecedent event (Abstract, L13-17; Cl2, L54-60).

KA does not expressly teach that the circuit transitions between states only on edges of a periodic clock signal supplied as input. **SE** teaches that the circuit transitions between states only on edges of a periodic clock signal supplied as input (CL8, L4-11 and L22-29; Cl9, L60-65), as that would allow the user to control the precise time of sampling signals from the target system by properly connected storage devices (CL10, L37-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **KA** with the method of **SE** that included the circuit transitioning between states only on edges of a periodic clock signal supplied as input, as that would allow the user to control the precise time of sampling signals from the target system by properly connected storage devices.

KA teaches the circuit output generated by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event (Abstract, L13-17; Cl2, L54-60). **KA** does not expressly teach the generated state space model includes all states of the circuit that are reachable from the current state of the circuit represented by the waveform data within the finite number of periods of the clock signal after the waveform data represents the antecedent event. **CH** teaches the generated state space model includes all states of the circuit that are reachable from the current state of the circuit (Abstract, L6-11 and L14-15; Fig 2, Blk 260), as that would allow the user to determine if a given specification produces

unexpected results (Abstract, L15-17); and as per **KA**, allow verifying that the design of the circuit meets specified operational correctness and performance criteria within specified time frames (Abstract, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **KA** with the method of **CH** that included the generated state space model including all states of the circuit that would be reachable from the current state of the circuit, as that would allow the user to determine if a given specification produced unexpected results; and allow verifying that the design of the circuit met specified operational correctness and performance criteria within specified time frames.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
November 24, 2003

HUGH JONES Ph.D.
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